

AMENDMENTS TO THE CLAIMS

Please amend claims 70-81 as indicated below.

Claims 1-38 (Cancelled)

39. (Previously Presented) A system comprising:

a processor;

a processor bus coupled to the processor;

a memory;

a memory control hub coupled to the processor bus and coupled to the memory;

a graphics accelerator coupled to the memory control hub;

a bus coupled to the memory control hub, the bus to transmit packets;

an input-output hub coupled to the bus and to couple to an input-output device,
wherein the system is capable of passing messages between the memory control
hub and the input-output hub through packets transmitted on the bus, the
messages including information about signals received from one or more of the
processor, the memory, and the input-output device,

wherein the bus is capable of using a source synchronous (SS) data transfer
technique that is capable of being quad-clocked.

Claims 40-46 (Cancelled)

47. (Previously Presented) A system comprising:

a first hub to receive a first signal;

a first hub interface coupled to the first hub, the first hub interface to receive a message that is passed from the first hub, the message corresponding to the first signal, the message including a packet including control information;

a second hub coupled to the first hub interface, the second hub to receive the message from the first hub interface,

wherein the packet including the control information comprises a special cycle packet embodying virtual wire control information.

48. (Previously Presented) The system of claim 47, wherein the virtual wire control information is in place of a wired sideband control.
49. (Previously Presented) The system of claim 47, wherein the packet including control information includes a special cycle packet encoding a command to assert a PHLD signal.
50. (Previously Presented) A system comprising:

a first hub to receive a first signal;

a first hub interface coupled to the first hub, the first hub interface to receive a message that is passed from the first hub, the message corresponding to the first signal, the message including a packet including control information;

a second hub coupled to the first hub interface, the second hub to receive the message from the first hub interface,

wherein the first hub interface is capable of using a source synchronous (SS) data transfer technique that is capable of being quad-clocked.

51. (Previously Presented) A system comprising:

a first hub to receive a first signal;

a first hub interface coupled to the first hub, the first hub interface to receive a message that is passed from the first hub, the message corresponding to the first signal, the message including a packet including control information;

a second hub coupled to the first hub interface, the second hub to receive the message from the first hub interface

a second hub interface coupled to the second hub, the second hub interface to receive the message from the second hub; and

a third hub coupled to the second hub interface to receive the message from the second hub interface, wherein the message includes control information to control the second hub and the third hub.

Claims 52-56 (Cancelled)

57. (Previously Presented) An apparatus comprising:

a first component;

a bus coupled to the first component, the bus to transmit packets, the packets including special cycle packets embodying control information; and

a second component coupled to the bus, the second component to receive the packets from the first component via the bus,

wherein the bus is capable of using a source synchronous (SS) data transfer technique that is capable of being multi-clocked.

58. (Previously Presented) The apparatus of claim 57, wherein the first component comprises a memory control hub, and wherein the second component comprises an input-output hub.
59. (Previously Presented) The apparatus of claim 58, further comprising:
- a graphics accelerator coupled to the first component; and
- a FLASH bios coupled to the second component.

Claims 60-66 (Cancelled)

67. (Previously Presented) A method comprising:
- receiving a first signal at a first hub coupled to a hub interface;
- passing a message corresponding to the first signal from the first hub through the first hub interface, the message including a packet including control information;
- and
- receiving the message from the hub interface at a second hub coupled to the hub interface,
- wherein the control information embodies virtual wire control information.
68. (Previously Presented) The method of claim 67, further comprising:
- checking the packet for a special cycle; and
- if a special cycle is found, then processing the special cycle.
69. (Previously Presented) A method comprising:
- receiving a first signal at a first hub coupled to a hub interface;

passing a message corresponding to the first signal from the first hub through the first hub interface, the message including a packet including control information;

receiving the message from the hub interface at a second hub coupled to the hub interface;

determining if the message is intended for the second hub;

acting on the message if said determining indicates the message is intended for the second hub; and

passing the message through a second hub interface if the determining indicates the message is not intended for the second hub.

70. (Currently Amended) The system of claim 47, wherein the [[packets comprise]] packet comprises a special cycle packet encoding a command to assert a PHLD signal.
71. (Currently Amended) The system of claim 47, wherein the [[packets comprise]] packet comprises a special cycle packet encoding a command to act as if SERR# was received.
72. (Currently Amended) The system of claim 47, [[wherein the]] further comprising a bus [[is]] capable of using a packet-based split-transaction protocol.
73. (Currently Amended) The system of claim 47, wherein the first [[component]] hub comprises a memory control hub, and wherein the second [[component]] hub comprises an input-output hub.
74. (Currently Amended) The system of claim 50, wherein the [[packets comprise]] packet comprises a special cycle packet encoding a command to assert a PHLD signal.

75. (Currently Amended) The system of claim 50, wherein the [[packets comprise]] packet comprises a special cycle packet encoding a command to act as if SERR# was received.
76. (Currently Amended) The system of claim 50, [[wherein the]] further comprising a bus [[is]] capable of using a packet-based split-transaction protocol.
77. (Currently Amended) The system of claim 50, wherein the first [[component]] hub comprises a memory control hub, and wherein the second [[component]] hub comprises an input-output hub.
78. (Currently Amended) The system of claim 51, wherein the [[packets comprise]] packet comprises a special cycle packet encoding a command to assert a PHLD signal.
79. (Currently Amended) The system of claim 51, wherein the [[packets comprise]] packet comprises a special cycle packet encoding a command to act as if SERR# was received.
80. (Currently Amended) The system of claim 51, [[wherein the]] further comprising a bus [[is]] capable of using a packet-based split-transaction protocol.
81. (Currently Amended) The system of claim 51, wherein the first [[component]] hub comprises a memory control hub, and wherein the second [[component]] hub comprises an input-output hub.